EE115C – Winter 2018
Digital Electronic Circuits
Mon & Wed 4:00-5:50pm
Boelter Hall Rm #2444
Personnel

♦ Instructor
  – Sudhakar Pamarti
  – 6731F Boelter Hall, (310) 825 2657, spamarti@ee.ucla.edu
  – Office Hours: MW 6:00pm – 7:00pm

♦ TA(s)
  – Szu-Yao Hung

♦ Reader(s)
  – TBD
Digital Integrated Circuits

- **Basics**
  - Transistor behavior and fabrication technology

- **Simple Static CMOS Logic Gate (Circuit) Design**
  - Delay, power analyses, transistor sizing, and layout

- **Interconnect (Wires)**
  - R and C

- **Combinatorial Logic Block Design**
  - Chain of logic gates
  - Delay analysis, sizing; logical effort

- **Sequential Logic Block Design**
  - Latches, flip-flops, timing analysis

- **Design and simulation experience**
  - Cadence software, generic CMOS process
Class Organization

- **6-7 homework assignments**
  - Due in class, see class web-site for schedule

- **1 design project**
  - Assigned in parts throughout the course
  - Finally due on Thursday, March 14, 2018, in class

- **Exams: midterm, final**
  - Midterm: Wednesday, Feb 14, 2018, 4:00pm – 5:50am, in class
  - Final: Monday, March 19, 2018, 8:00am – 11:00am, Location TBD
Grading Policy

- Homework: 15%
- Project: 24%
- Midterm: 25%
- Final: 35%
- Survey: 1%

- No collaboration allowed unless explicitly specified
Class Material


❖ CAD software
   - Cadence IC design suite
   - Tool setup instructions and tutorials will be posted online